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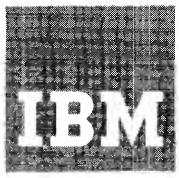

Systems Reference Library

# IBM 7094 Model II Data Processing System

This announcement bulletin provides information about the IBM 7094-II Data Processing System. It contains a generalized description of the main features of this system, together with a sample instruction sequence and rules for the application of extended sequence overlap operations. A listing of instruction cycle changes, as well as a table of instructions capable of being overlapped, is included.

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Increased computational speed, coupled with faster throughput, is provided in the newest addition to IBM data processing systems -- the 7094-II. Designed to meet growth requirements for IBM 7090/7094 users, the 7094-II maintains compatibility of programming and data assignments, input/output and random storage configurations, and operations with the 7094.

The salient features of this new system are:

--- reduced core storage cycle time
--- extended sequence overlap operations
--- reduction in cycle times for certain arithmetic operations

Core storage cycle time, together with the basic machine cycle, has been reduced from 2.0 microseconds to 1.4 microseconds.

Extended sequence overlap has been combined with the faster access time, resulting in substantial increases in internal performance.

Average execution times of fixed and floating point multiply and divide instructions have been reduced by one cycle.

The various units of the IBM 7094-II remain the same as for the 7090/7094 with the following exceptions:

The IBM 7302 Model 3 Core Storage unit replaces the IBM 7302 Core Storage unit, the IBM 7111 Instruction Processing unit replaces the IBM 7108 (in 7090) or the IBM 7110 (in 7094), and the IBM 7606 Model 2 Multiplexor is used in place of the IBM 7606 Model 1 Multiplexor.

## OPERATION

Essential to 7094-II operation are two logically independent core storage arrays, each consisting of 16K, 36-bit words with a cycle time of 1.4 microseconds. Two words can be referenced simultaneously, one word in the even array, the other in the odd array. Two words (not necessarily in consecutive locations) can be obtained from storage at the same time, or one word can be obtained while the other word is being stored. Simultaneous store operations are not performed.

The 7094-II can execute a continual flow of overlapped instructions until the sequence of instructions is terminated. This differs from the double instruction overlap in the 7094 where sequences of only two instructions are overlapped. When the 7094 completes such a sequence, it is then possible to achieve overlap in the next two-instruction pair; but overlap between pairs is not possible.

In the extended sequence overlap operation of the 7094-II, long sequences of instructions can be executed with the resultant elimination of all I cycles, except the I cycle of the initial instruction of the sequence. This is accomplished by overlapping the I cycle with the E or L cycle of the preceding instruction.

Two conditions can cause extended sequence overlap to be temporarily suspended. First, certain combinations of the two instructions brought simultaneously from core storage may, by the nature of the instructions, preclude overlap operations; these instructions are listed in Table I. Second, a storage conflict will occur if an address in the operand of the preceding instruction refers to the same core array as the location of the current instruction, that is, if both refer to the even core array or both to the odd core array.

## IBM 7094-II INSTRUCTION CYCLES

The instructions provided in the 7094-II are exactly the same as in the 7094; however, cycle time for instructions has been reduced to 1.4 microseconds. In addition, the number of cycles required by the following instructions has been changed as follows:

| Instruction | 7094 II Cycles | Average |
|---|---|---|
| FMP, UFM, MPY, MPR | 2-4 | 4 |
| FDP, FDH | 2-6 | 6 |
| DVP, DVH | 2-7 | 7 |
| DFMP, DUFM | 2-9 | 9 |
| DFDP, DFDH | 2-13 | 13 |
| VDH, VDP | 2-7 | - |
| VLM | 2-4 | - |
| LLS, LRS, LGL, LGR | 2-6 | - |
| ALS, ARS, RQL | 2-4 | - |
| SCHX | 2-3 | - |
| ENB | 3-4 | - |
| RCHX, LCHX | 4-5 | - |
| RDS, WRS, BSR, WEF, REW, RUN, SDN | 2-3 | - |
| RDS, WRS, (Card Machines) | 3-4 | - |
| ETT, BTT, TEF, TRC | 3-4 | - |
| TCOX, TCNX | 2 | - |

The number of cycles required for a given sequence of instructions is determined by adding up the total number of cycles involved, and subtracting the number of I cycles that can be processed concurrently with the E or L cycle of each preceding instruction. The following rule specifies condition of overlap. The I time for the current instruction need not be counted if (and only if):

1. The current instruction can have its I time overlapped (as shown in Table I), and

2. The preceding instruction can have its E (or L) time overlapped, and
3. No storage conflict occurs. This will be the case if (and only if) any of the following occurs:
   a) The preceding instruction requires at least one L cycle.
   b) The I time of the preceding instruction was not eliminated due to overlap.
   c) The location of the current instruction and the data referenced by the preceding instruction are in different core arrays.

The following instruction sequence illustrates the application of this rule.

| Operation | Cycles Required |
|---|---|
| LDQ | IE |
| FMP | (I)ELL |
| FAD | (I)EL |
| STO | (I)E |
| TIX | (I) |

The cycles enclosed in parentheses may be eliminated. Conditions 1 and 2 hold for all instructions; only condition 3 is involved in the following:

FMP: Rule 3b is satisfied. I time of the previous instruction, LDQ, was not eliminated.

FAD: Rule 3a is satisfied. The preceding instruction, FMP, had an L cycle.

STO: Rule 3a is satisfied. The preceding instruction, FAD, had an L cycle.

TIX: Neither 3a nor 3b is satisfied. Elimination of the I cycle will occur only if the TIX and the data required by the STO are in different logical storage arrays.

When different storage arrays are used, the total number of cycles required for this sample instruction sequence is eight 1.4 microsecond cycles. The same instruction sequence on the 7094 would be executed as follows:

1. The FMP instruction requires an additional L cycle.
2. Either one or two I cycles are overlapped, depending upon whether the first instruction is located at an odd or even storage array.

The sample instruction sequence, if processed on a 7094, requires eleven 2-microsecond cycles.

Table I. Listing of Instructions -- Overlap Activity

| I Cycle Can Be Overlapped | E or L Cycle Can Be Overlapped | Instructions | Cycles |
|---|---|---|---|
| | | IIS, OSI, RIS, LDI | I, E |
| | | SIR, SIL, RIR, RIL | I |
| | | RIA, PAI, PIA, OAI | I |
| | | TIO, TIF | I, L |
| X | | PXA, PXD, PCA, PCD | I |
| X | | PDC, PDX, PAX, PAC | I |
| X | | TSX | I |
| X | | TIX, TNX, TXL, TXH, TXI | I |
| X | | DLD | I, E |
| X | X | STO, STQ, STZ, SLW, STI | I, E |
| X | X | SLQ | I, E |
| X | X | ADD, ADM, SUB, SBM | I, E |
| X | X | DST | I, E, E |
| X | X | STP, STO, STT, STA | I, E |
| X | X | CLA, CLS, CAL | I, E |
| X | X | SXA, SCA, SXD, SCD | I, E |
| X | X | STL | I, E |
| X | | XCL | I |
| X | | XCA | I |
| X | | ZET | I, E |
| X | | AXT, AXC | I |
| X | | LXA, LXD, LAC, LDC | I, E |
| | | TNZ, TZE | I |
| | | TLQ | I, L |
| | | TQP, TPL, TMI, TOV, TNO, TQO | I |
| | | PSE | I, L |
| | | PBT, LBT, DCT | I, L |
| | | MSE | I, L |
| | | ETM, LTM | I, L |
| X | | ACL | I, E |
| | | RND, CLM, COM | I, L |
| | | EFTM, LFTM, ESTM, ECTM, LSNM | I, L |
| | | TCO, TCN | I |
| | | ANA | I, E, L |
| | | ANS | I, E, L, E |
| | | CVR, CRQ, CAQ | I, L, E ----- |
| X | | ERA | I, E, L |
| | | SSM, SSP, CHS | I, L |
| | | ENK | I, L |
| X | X | LDQ | I, E |
| X | | TRA, TTR, ESNT | I |
| | | HTR | I, L --- |
| X | X | RQL | I, L --- |
| X | X | ALS, ARS, LLS, LRS, LGL, LGR | I, L --- |
| X | X | CAS, LAS | I, E |
| | | LFT, LNT, RFT, RNT | I, L, L |
| | | OFT, ONT | I, E, L, L |
| | | IIA, IIL, IIR | I |
| X | X | FAD, FAM, FSB, FSM | I, E, L --- |
| X | X | FMP, UFM, MPY | I, E, L, L |
| X | X | MPR | I, E, L, L, L |
| X | X | FDP, FDH | I, E, 4L |
| X | X | DVP | I, E, 5L |
| X | | DVH | I, E, 5L |
| X | | DFMP, DUFM | I, E, 7L |
| X | | DFDP, DFDH | I, E, 11L |
| X | X | VDP | I, E, L -- |
| X | | VDH | I, E, L -- |
| X | X | VLM | I, E, L- |

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